

EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|-------|------|---|--|------------------|---------|------------------|
| L1 | 9 | ("6,721,271") or ("6,667,956") or ("6,646,986") or ("6,580,721") or ("6,404,735") or ("6,393,590") or ("6,356,546") or ("6,088,331") or ("6,041,040")).PN. | US-PGPUB; USPAT | OR | OFF | 2006/07/28 09:23 |
| L2 | 50 | ((bus controller) with (arbitrat\$3) same priority) same ((count\$2 value weight\$3) near3 (increment\$3 decrement\$3 increas\$3 decreas\$3 add\$3 subtract\$3)) same (interval cycle period) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L3 | 539 | (718/103).CCLS. | US-PGPUB; USPAT | OR | OFF | 2006/07/28 10:34 |
| L4 | 1129 | (718/104).CCLS. | US-PGPUB; USPAT | OR | OFF | 2006/07/28 10:34 |
| L5 | 494 | (access\$3 with priority with (process thread task) with (memory)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L6 | 28 | (access\$3 with priority with (process thread task) with counter) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L7 | 1992 | (access\$3 with priority with (process thread task)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L8 | 34 | (access\$3 with priority with (process thread task)) same (increment\$6 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L9 | 34 | (access\$3 with priority with (process thread task)) same (increment\$6 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L10 | 28 | (access\$3 with priority with counter with (process thread task)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L11 | 412 | (access\$3 with priority with counter) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L12 | 27 | (arbitrat\$3) same priority same ((count\$2 value weight\$3) near3 (increment\$3 decrement\$3 increas\$3 decreas\$3 add\$3 subtract\$3)) same (interval cycle period) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |

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| L13 | 25 | (process thread task) with (access\$3) near (resource memory) with (counter value variable) with (decreas\$3 subtract\$3 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L14 | 62 | (process thread task) with (access\$3) near (resource memory) with (counter value variable) with (increment\$6 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L15 | 4 | (process thread task) with (access\$3) near2 (resource memory) with (bandwidth) with (decreas\$3 subtract\$3 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L16 | 30 | (process thread task) with (access\$3) near2 (resource memory) with (counter value variable) with (decreas\$3 subtract\$3 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L17 | 347 | (process thread task) with (access\$3) with (counter value variable) with (increment\$6 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L18 | 190 | (thread process task) same priority same ((count\$2 value weight\$3 variable) near3 (decrement\$3 decreas\$3 subtract\$3)) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L19 | 190 | (thread process task) same priority same ((count\$2 value weight\$3 variable) near3 (decrement\$3 decreas\$3 subtract\$3)) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L20 | 0 | (thread process task) with access\$3 adj3 (memory resource) same priority same ((count\$2 value weight\$3 variable) near3 (decrement\$3 decreas\$3 subtract\$3)) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L21 | 0 | (thread process task) with access\$3 same priority same ((count\$2 value weight\$3 variable) near3 (decrement\$3 decreas\$3 subtract\$3)) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L22 | 6 | (thread process task) with priority with ((count\$2 value weight\$3 variable) near3 (decrement\$3 decreas\$3 subtract\$3)) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L23 | 319 | (thread process task) with priority with (count\$2 value weight\$3 variable) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |

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| L24 | 11 | (thread process task) with priority with (count\$2 value weight\$3 variable) with (decrement\$4 decreas\$3 subtract\$3) same (frequen\$4 rate) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L25 | 355 | (thread process task) with schedul\$4 with (counter) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L26 | 220 | (thread process) with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L27 | 7 | (thread process) with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) near2 counter | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L28 | 0 | (thread process) with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) same arbitration | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L29 | 32 | (thread process) with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) with (variable value counter) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L30 | 14 | (thread process) with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) with (variable value counter) and priority | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L31 | 0 | (thread process) with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) with arbitration | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L32 | 8 | (thread process) with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) with counter | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L33 | 6 | (thread process) with schedul\$4 with (burst time adj slice quantum) with (decrement\$4 decreas\$3 subtract\$3) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L34 | 8 | (US-6684280-\$ or US-5884051-\$ or US-5339443-\$ or US-5935234-\$ or US-5193197-\$ or US-6363445-\$ or US-6154769-\$).did. or (US-20020143843-\$).did. | US-PGPUB; USPAT | OR | OFF | 2006/07/28 10:34 |

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| L35 | 982 | access adj counter | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L36 | 154 | access adj counter same (process thread) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L37 | 44 | access adj counter same (process thread) same (increment\$4 decrement\$4) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L38 | 282 | access adj cycle same priority | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L39 | 4 | access adj cycle same priority same (counter value) near2 access\$3 | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L40 | 41 | count\$2 with (increment\$3 decrement\$3 increas\$3 decreas\$3 add\$3 subtract\$3) and priority same (shar\$3 near2 (resource memory computer)) same (access\$3 near3 (interval cycle period)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L41 | 1091 | memory adj controller with arbitrat\$3 | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L42 | 3 | memory adj controller with arbitrat\$3 with (decrement\$3 decreas\$3 substract\$3) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L43 | 0 | memory adj controller with arbitrat\$3 with (decrement\$3 decreas\$3 substract\$3) near2 counter | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L44 | 0 | memory adj controller with arbitrat\$3 with (decrement\$3 decreas\$3 substract\$3) with counter | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L45 | 131 | memory adj controller with arbitrat\$3 with priority | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |

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| L46 | 1 | memory adj controller with arbitrat\$3 with priority with (thread process) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L47 | 1129 | (718/104).CCLS. | US-PGPUB; USPAT | OR | OFF | 2006/07/28 10:34 |
| L48 | 0 | L47 and (access\$3 with priority with counter) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L49 | 539 | (718/103).CCLS. | US-PGPUB; USPAT | OR | OFF | 2006/07/28 10:34 |
| L50 | 4 | L49 and (access\$3 with priority with counter) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L51 | 412 | (access\$3 with priority with counter) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L52 | 291 | L51 and (((@ad < "20010126") or (@prad < "20010126") or (@rlad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L53 | 236 | L51 and (((@ad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L54 | 28 | (access\$3 with priority with counter with (process thread task)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L55 | 34 | (access\$3 with priority with (process thread task)) same (increment\$6 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L56 | 33 | L55 not L54 | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L57 | 494 | (access\$3 with priority with (process thread task) with (memory)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |

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| L58 | 362 | L57 and (((@ad < "20010126") or (@prad < "20010126") or (@rlad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L59 | 308 | L57 and (((@ad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L60 | 62 | (process thread task) with (access\$3) near (resource memory) with (counter value variable) with (increment\$6 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L61 | 31 | L60 and (((@ad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L62 | 25 | (process thread task) with (access\$3) near (resource memory) with (counter value variable) with (decreas\$3 subtract\$3 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L63 | 14 | L62 and (((@ad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L64 | 30 | (process thread task) with (access\$3) near2 (resource memory) with (counter value variable) with (decreas\$3 subtract\$3 decrement\$6) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L65 | 15 | L64 and (((@ad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L66 | 14 | L62 and (((@ad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L67 | 15 | L64 and (((@ad < "20010126"))) | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |
| L68 | 1 | L67 not L66 | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 10:34 |

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| L75 | 23 | (access\$3 same cycle same priority same resource).clm. | US-PGPUB; USPAT; USOCR; EPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/28 11:08 |
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arbitration unit. To start a bus cycle, the request line is asserted. ... reduce shared memory access in several ways. The first time a ...
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of the same priority merely. requires placing the program counter on the stack and ... match it to the appropriate. **access cycle** of the PPE shared. **memory**. ...
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Non-uniform **memory access** times. The cost of Concert has ... **priority order**. Indeed, we are studying other **arbitration** algorithms, ...
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arbitration cycle. Initially, each initi- ator's **priority** is set to its slot number. ... **memory**. The other **memory** is. **shared** between use as command reg- ...
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count through a **priority counter** to maintain. a rotating ... uga, **access requests** from an input port to the **shared**. buffer **memory** never block because any ...
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Use of **shared memory** as the principal medium for interproccssor. comllunication. ... **priority order**. Indeed, we are studying other **arbitration** algorithms, ...
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bus arbitration discipline [JOR74]. Although a fixed-priority ... **memory** having about 300 ns **access** time and 500 ns **read cycle** time. ...
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been granted **access** for a queued cell, it performs no other. checks for the remainder of the **arbitration cycle**, since each ...
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Since the **arbitration**. is per-. formed once every orthogonal **memory cycle** (the time. to transfer 16 data elements), the **access control board** ...
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cycle., it was necessary. to establish. a. **priority**. for these. transfers. ... **interconnection**. in the **memory**. path. A distributed. **arbitration** ...
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nication needs come from **shared access** to this ... **cycle** basis then **access** to this **memory** will be ... well as **priority** request signal. They are arran- ...

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counter is thus decremented each **cycle**. This mode is suitable ... is due to **arbitration** on. **shared resources** such as **access to memory** and monitors. This ...

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cycle, we **access** each of the **memory banks'** address registers. individually. No **arbitration** is necessary, since the paths of the. addresses will never cross. ...

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cution engine and the issues that arise with respect to **shared** ... following components: (1) path PC **arbitration** to gain **access**. to the instruction cache, ...

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idle, it has a higher **priority** in this **arbitration** than a busy output port. ... P. Vatsolaki, and A. Ethymiou, "Pipelined **Memory Shared** Buffer for VLSI ...

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sources with little interaction and coordinated **arbitration**. ... 1 port, seqeuntial **access**. **Shared L2**. 4MB, 32-way, 64B blocks, 51 **cycle** hit, LRU ...

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access time of the dynamic RAMs used to build the **memory**. The **memory** architecture of ... into a single execution **cycle**, we must establish a **priority** rela- ...

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with a **shared memory** through a GREEDY network and synchronized ... **memory**. **cycle** and the data on which this **arbitration** must be performed ...

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register file with multi-**cycle** **access** time would increase. branch misprediction penalty since a ... implement synchronous counters and **priority arbitration**. ...

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having top **priority**. With smart **arbitration** the round. robin will not "advance" if, for example, ... **Shared Memory Parallel Computer**.". IEEE Tranracfions ...

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pipeline stages, the average **memory cycle** time degradation equals the ... as follows:

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case, agents follow the assured **access** protocol for non-priority requests, but ignore the protocol and compete in every arbitration for **priority** requests. ...
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are usually connected by a **shared** serial media, the underlying communication platform is the ... multiple access (TDMA) **arbitration** scheme, where each ...
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kernel patches and **priority** scheduling, TCPivo can be made highly resilient to background ... **access** to the **shared memory**. Both can limit the maximum ...
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their output onto the **arbitration** bus and thence out of the module. ... The Instruction Store comprises a random-access **memory** and two registers. ...
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injection to the FSB to lengthen (dilate) the host **memory access** ... During the **arbitration** phase the FSB protocol selects (among ...
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shared memory programming model is made possible by a patented new architectural technique ... board that handles **arbitration** and **access** to the bus. ...
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token **arbitration** where only one unit can do a task at a time. ... tional Symposium on **Shared Memory Multiprocessors**. (sponsored by ...
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bus **cycle** time violations, while synthesizing a feasible, low-cost ... **arbitration** priority orderings, data bus widths, bus clock speeds and DMA ...
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on busses with **priority arbitration** logic. 2'3 ... microprogrammable minicomputer, and **access**. to a large virtual **memory**. This **memory** can ...

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The bus select and **arbitration** logic allows both processors to **access** a common **memory**(iKx16 bits RAM). Only one processor can **access** this common **memory** at a ...

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memory is in the **access** of semaphores protecting **shared** data ... functions of a bus controller such as bus **arbitration** and system. clock control. ...

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can **access** the **shared**. **memory** directly through the 32-bit data and ... **arbitration**. is managed by the MC68452. bus. **arbitration**. unit and the RS232 ...

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During each **arbitration** **cycle**, a queue handler that wishes to ... **Shared** **memory**

was used for communication between parts. of the system. ...

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memory **shared** buffer for VLSI switches. In Proc. Confer- ... An enhanced **access** and **cycle**. time model for on-chip caches. Technical Report 93/5, DEC ...

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formance because it controls **access** to the **shared** bus. and **memory**. The arbiter simulations ... ers and software developers early in the design **cycle**. ...

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nanosecond microinstruction **cycle** time, a high speed cache, **memory** ... and using a **shared** bus or a switch to **access** the **memory**, the Dorado ...

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mits the processor's interrupt **arbitration** logic to determin- ... **shared** **memory** and network inputs that were computed us- ing a genetic algorithm. ...

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scheduler thread via scheduler command queues in **shared** **memory** that interrupt the scheduler loop ... L2 hit time includes **arbitration** and bus transfer time. ...

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two highest **priority** threads whose fetches are not blocked. We also prioritize the **arbitration** for **shared** resources each. **cycle** to favor the higher-**priority** ...

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The **memory** system supports a tightly coupled, shared processor structure. ... addresses, permitting single **cycle access**. Due to the high ...
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During the second half **cycle**, the micro- program address for the highest **priority** task is fetched from the task specific program **counter TPC**. ...
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have to endure a full L2 to main **memory request cycle**; the pointer ... each **memory request**, with this **priority** being used during **memory bus arbitration**. ...
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which of the following methods of **arbitration**, or **priority resolution** can resolve the **priority** at ... nificant lowering of the **memory access time** at ...
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22ns **snoop cycle** (including 2 ns **arbitration**). pipelined, point-to-point crossbar ... approach to exclusive data **access** in shared **memory** multi- processors. ...
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similar to the transactional **memory** proposed in [6]. It is a general hardware mechanism to support lock free atomic **access** to shared data structures. ...
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standard hardware design **cycle**. In order to do so, the technology ... the second project, a distributed **shared-memory** MESI cache co- ...
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RuleBase presents **counter-examples** and **witnesses** (see below) as timing diagrams. ... the second project, a distributed **shared-memory** MESI cache co- ...
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of the network largely establish the remote **memory access**, latency and bandwidth. ... switch **arbitration** is done speculatively. Each **cycle**, each ...
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shared by all **memory** modules (see figure 2). Bus **arbitration** takes one **cycle**. Transmitting the request to a **memory** module requires exclusive bus **access** ...
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lock bits on the **shared memory**, and **access** them with atomic test-and-set ... mined from the **access** pattern is 5%. Fixed-priority bus **arbitration** ...
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controller and using a **shared bus** or a switch to access the. **memory** ... **priority** encoding and reading of TPC, into. one **cycle** is quite difficult. these two ... portal.acm.org/ft_gateway.cfm?id=285978& type=pdf&coll=ACM&dl=ACM&CFID=15151515&CFTOK... - [Similar pages](#)

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shared basis, with the IOC having the **priority**. After the. command instruction, the CP suspends its ... **memory** module has a fixed **cycle** time that depends on ... portal.acm.org/ft_gateway.cfm?id=306866& type=pdf&coll=GUIDE&dl=GUIDE&CFID=15151515&CF... - [Similar pages](#)

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hierarchy to reduce the effective memory access time. The memory hierarchy of a shared-memory multiprocessor can be further optimized by (1) ...
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